

Figure 1a

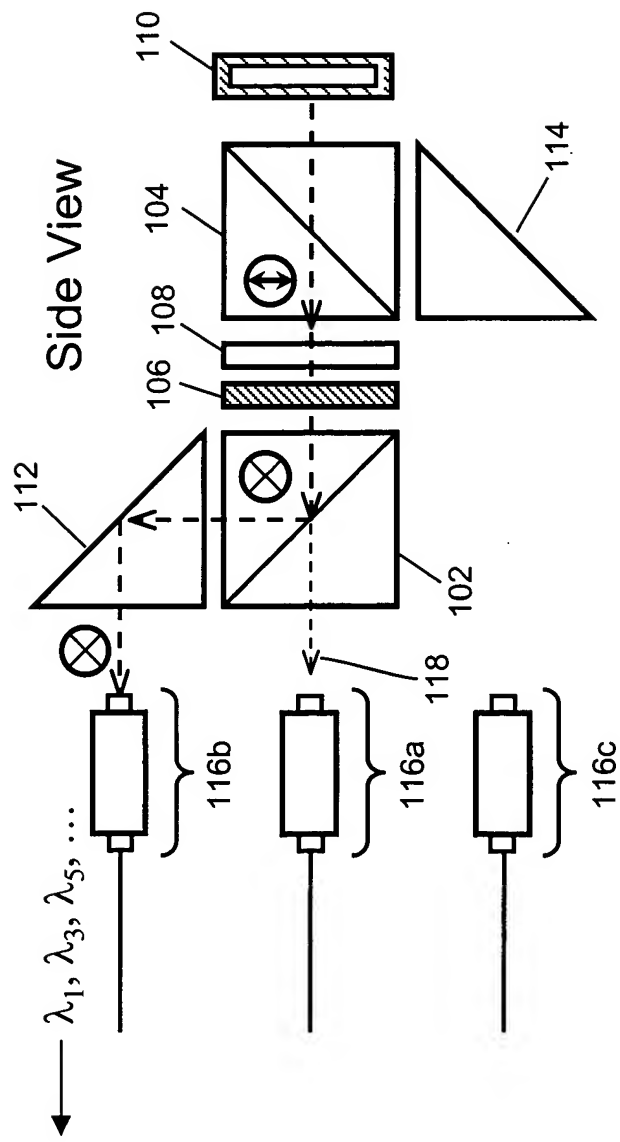
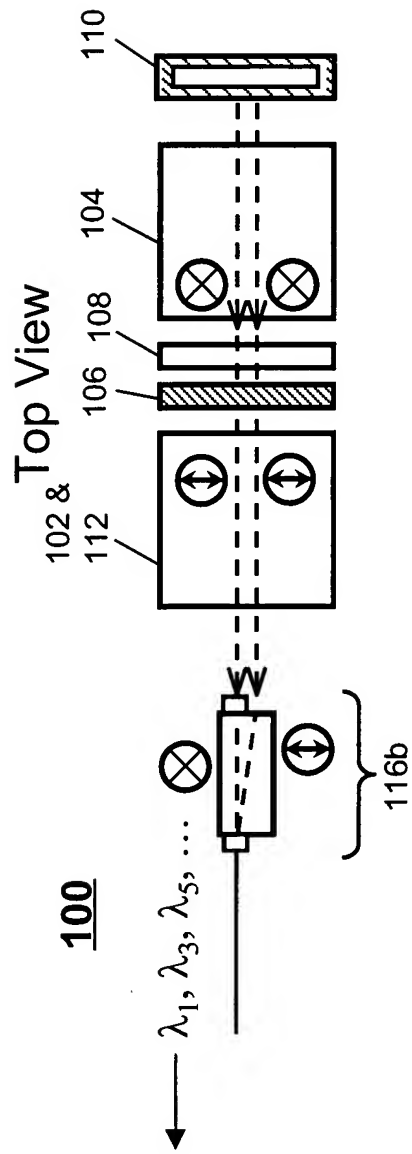


Figure 1b

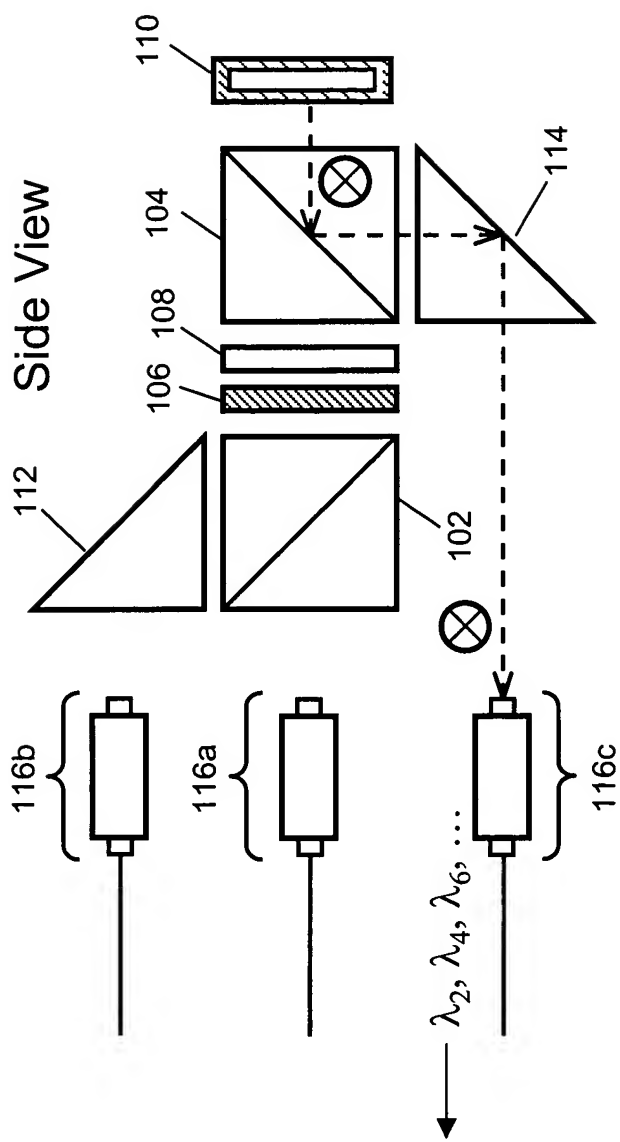
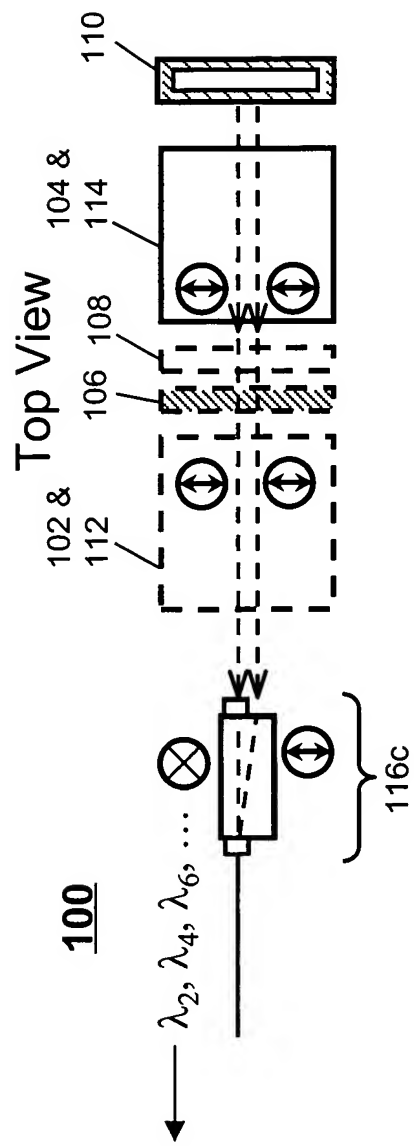


Figure 1c

116

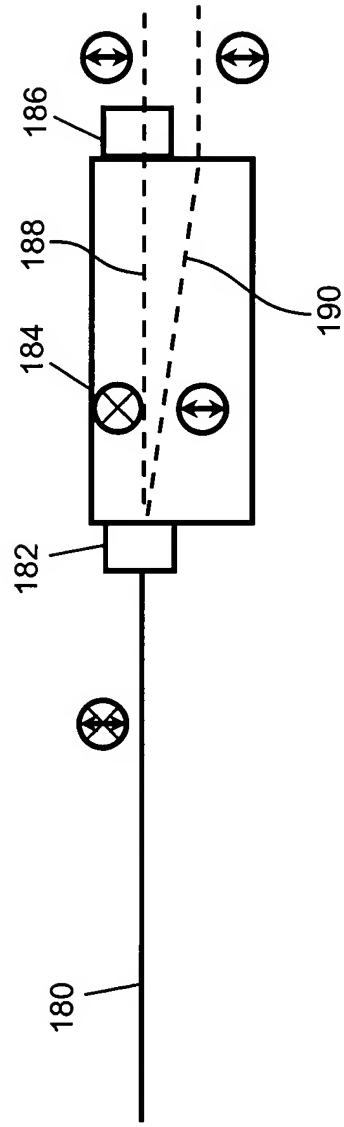


Figure 1d

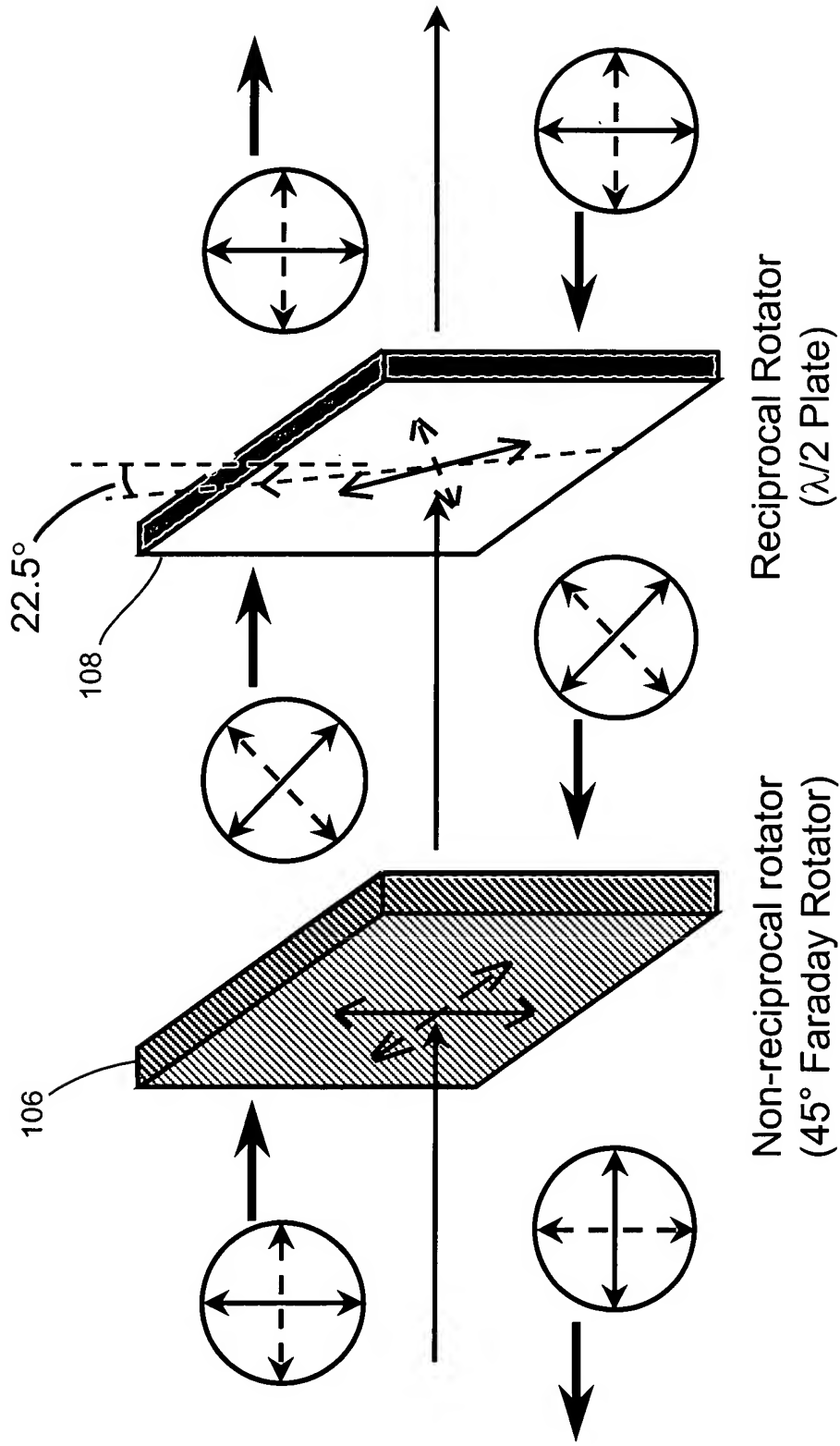


Figure 1f
(Prior Art)

200

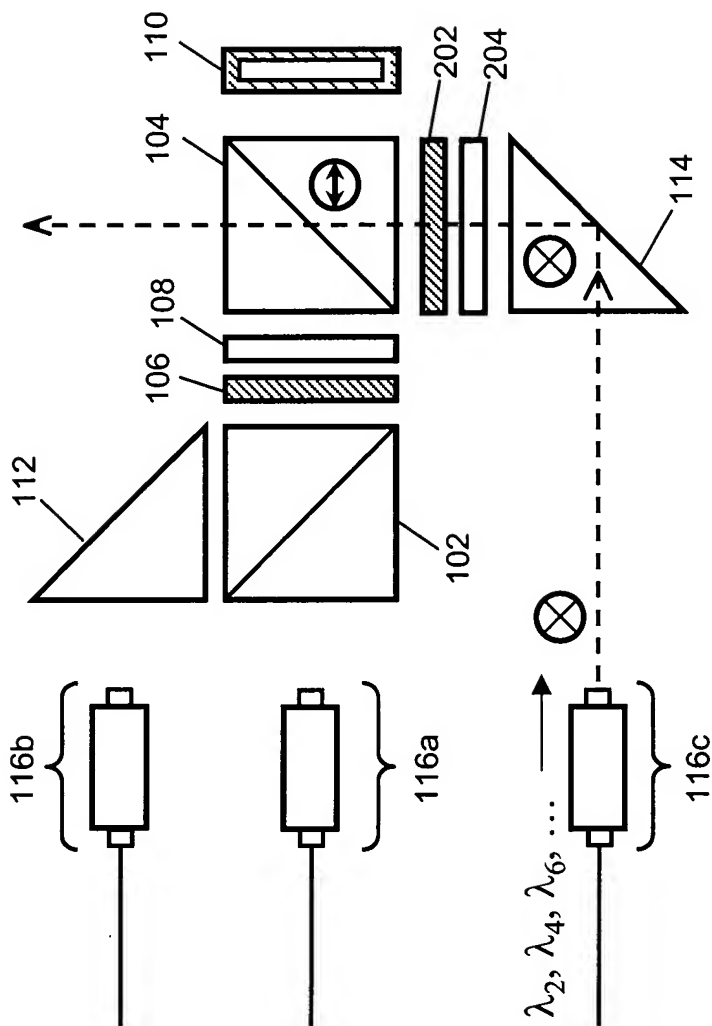


Figure 2a

200

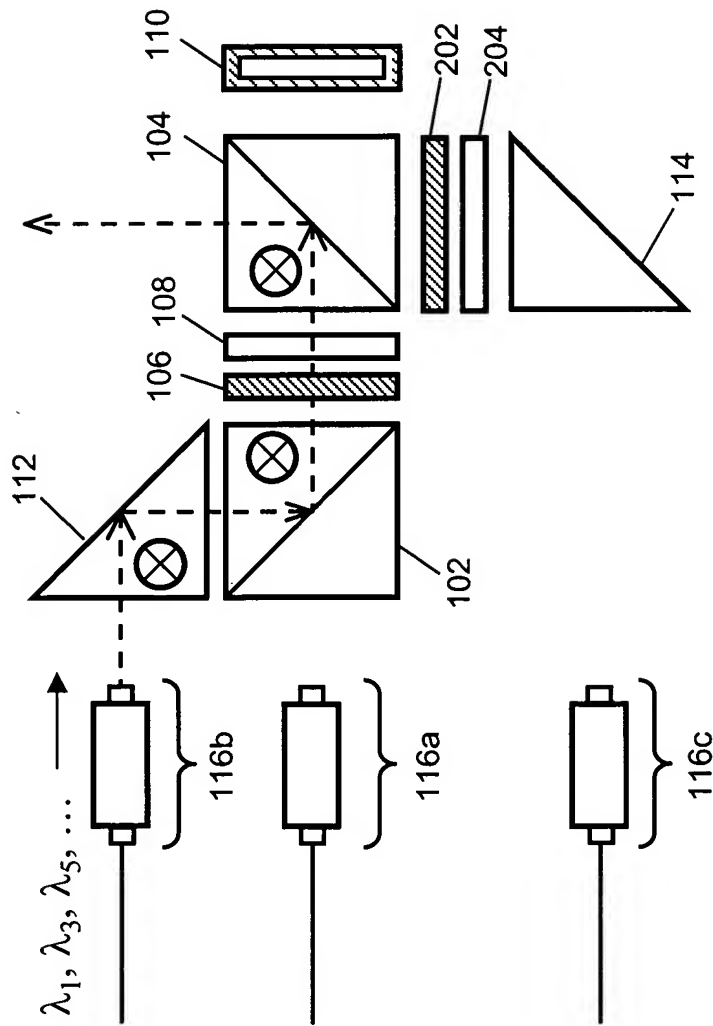


Figure 2b

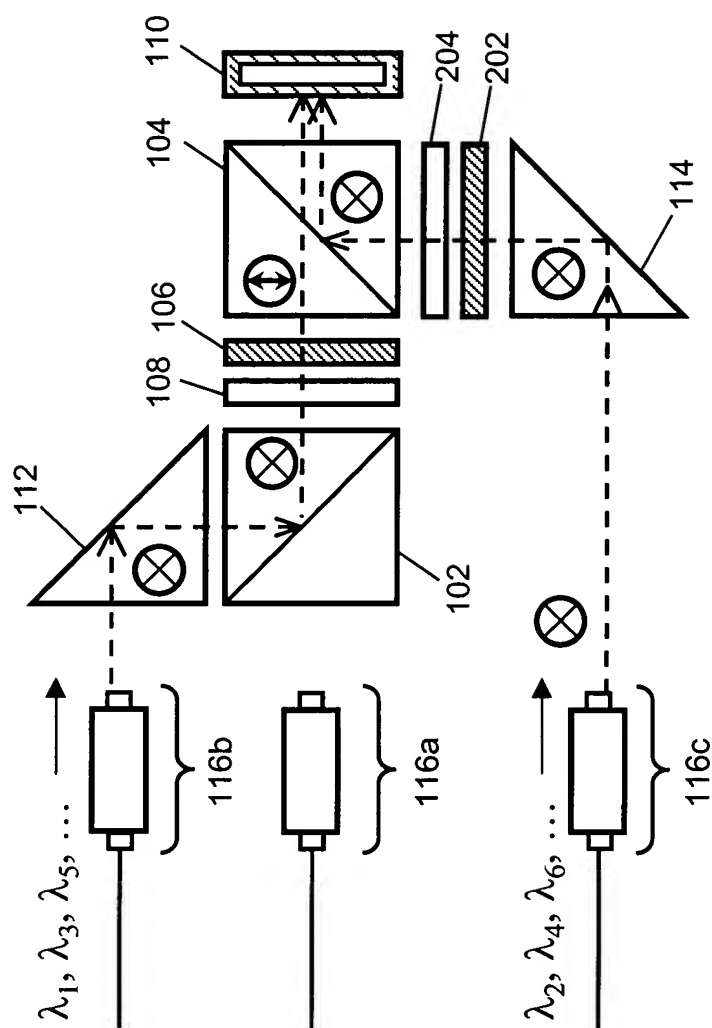


Figure 4a

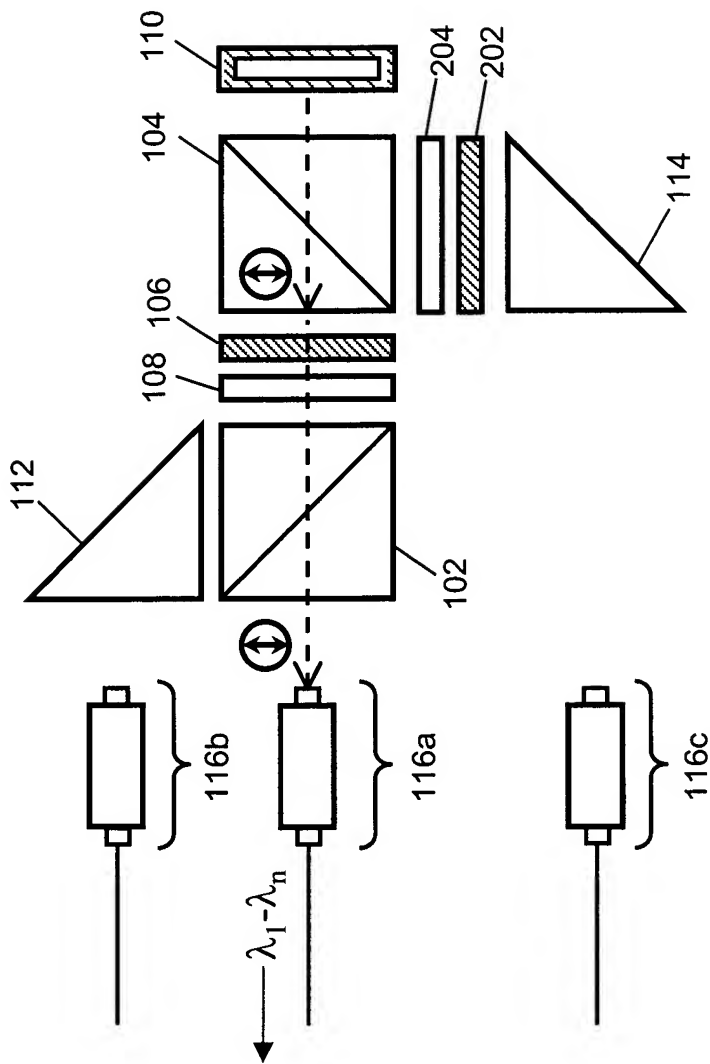


Figure 4b

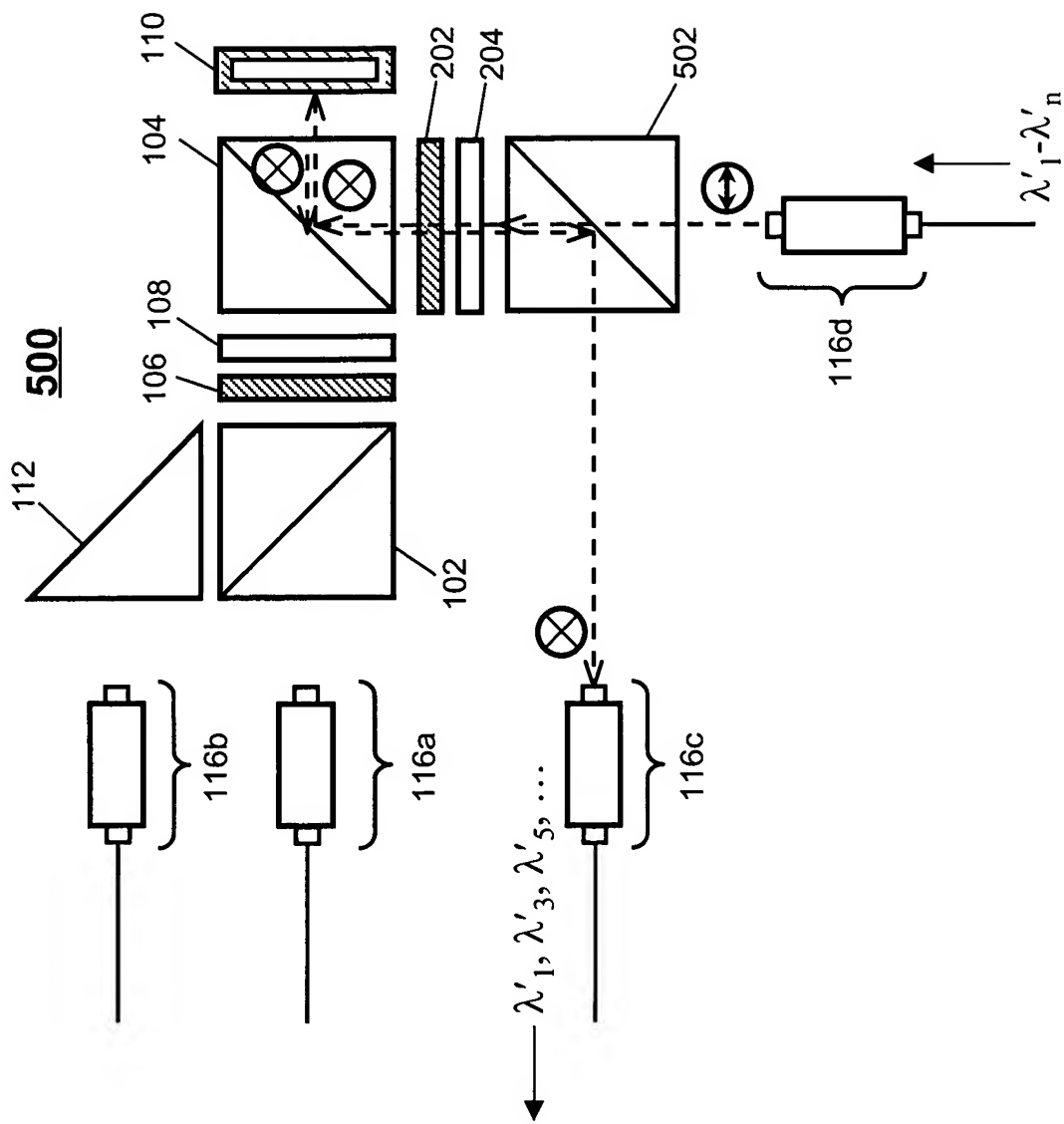


Figure 5a

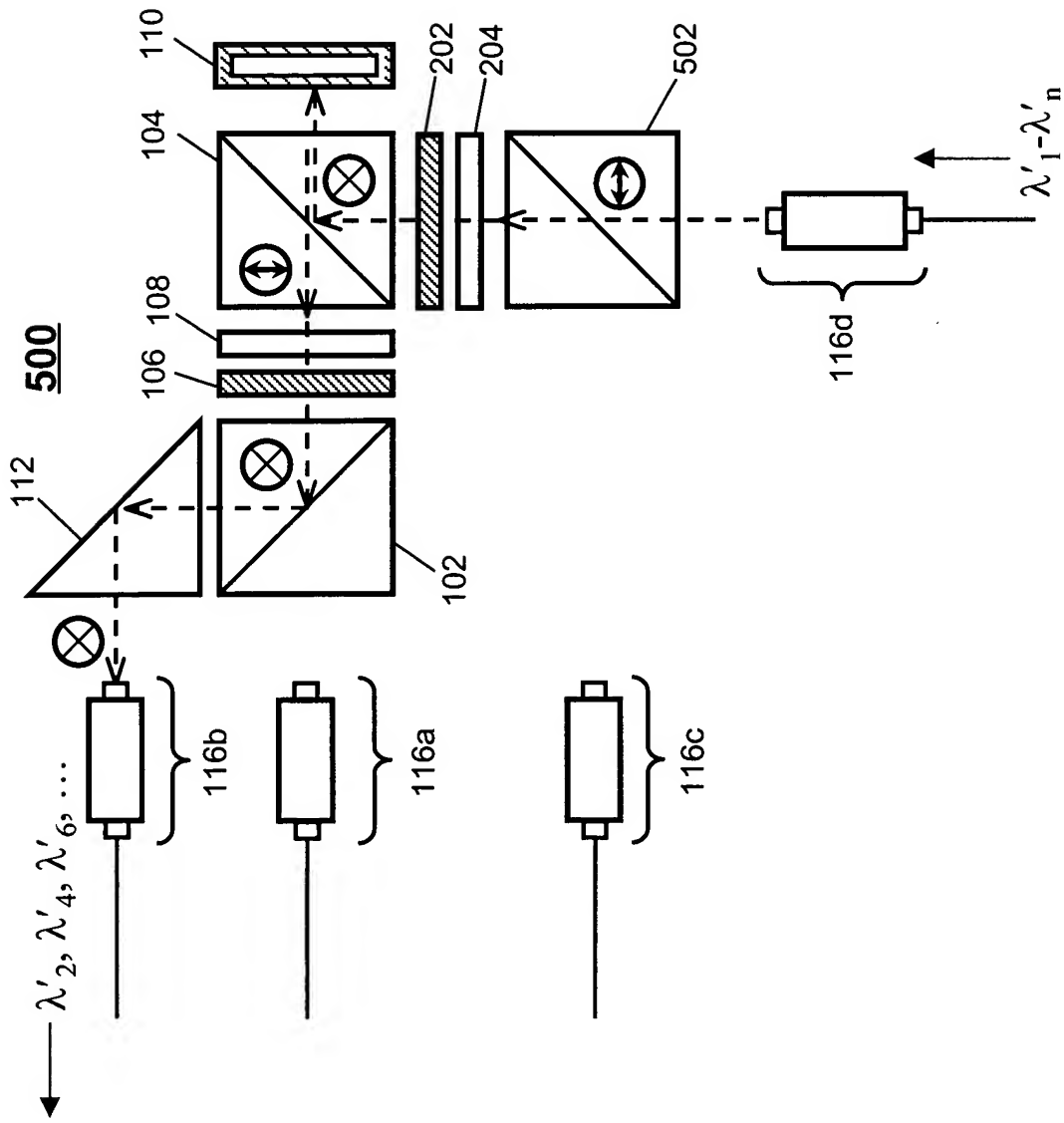


Figure 5b

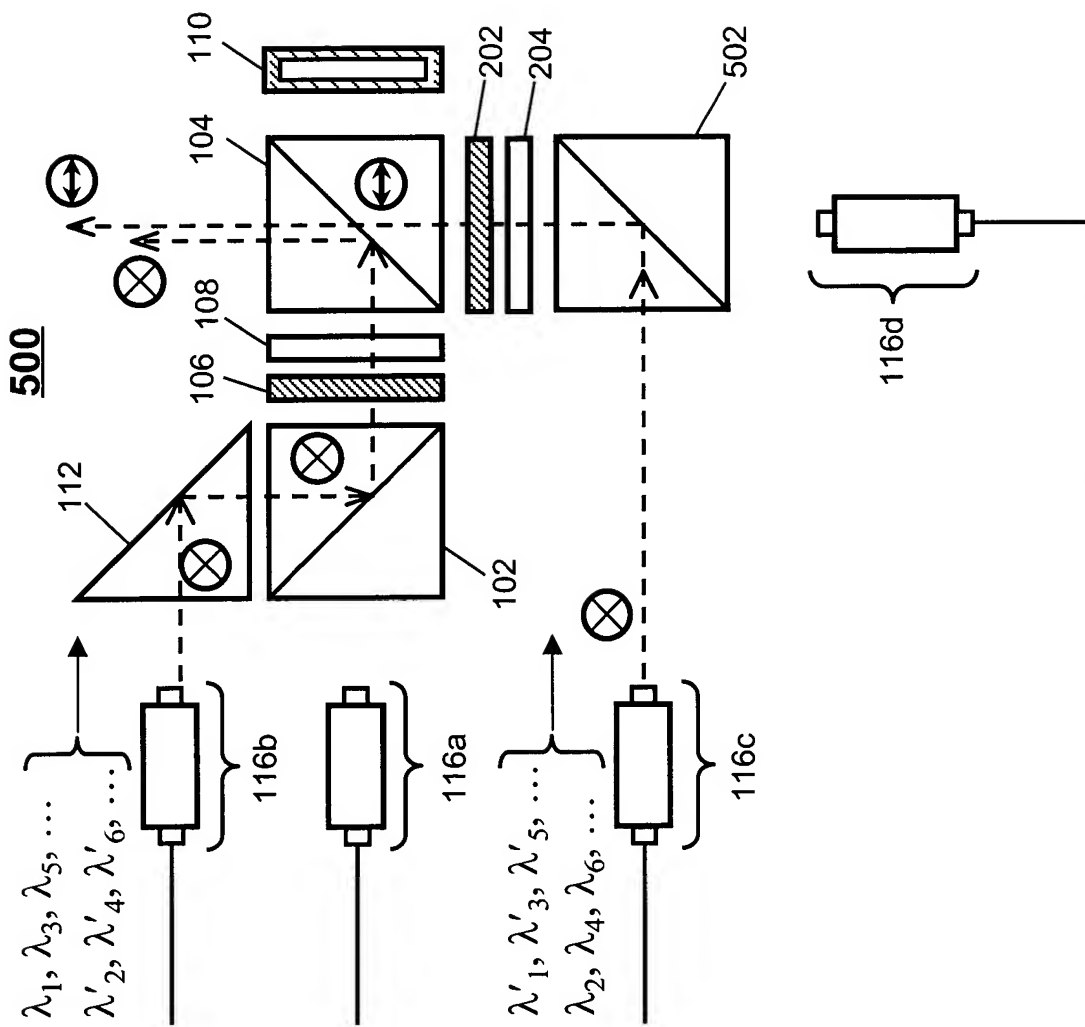
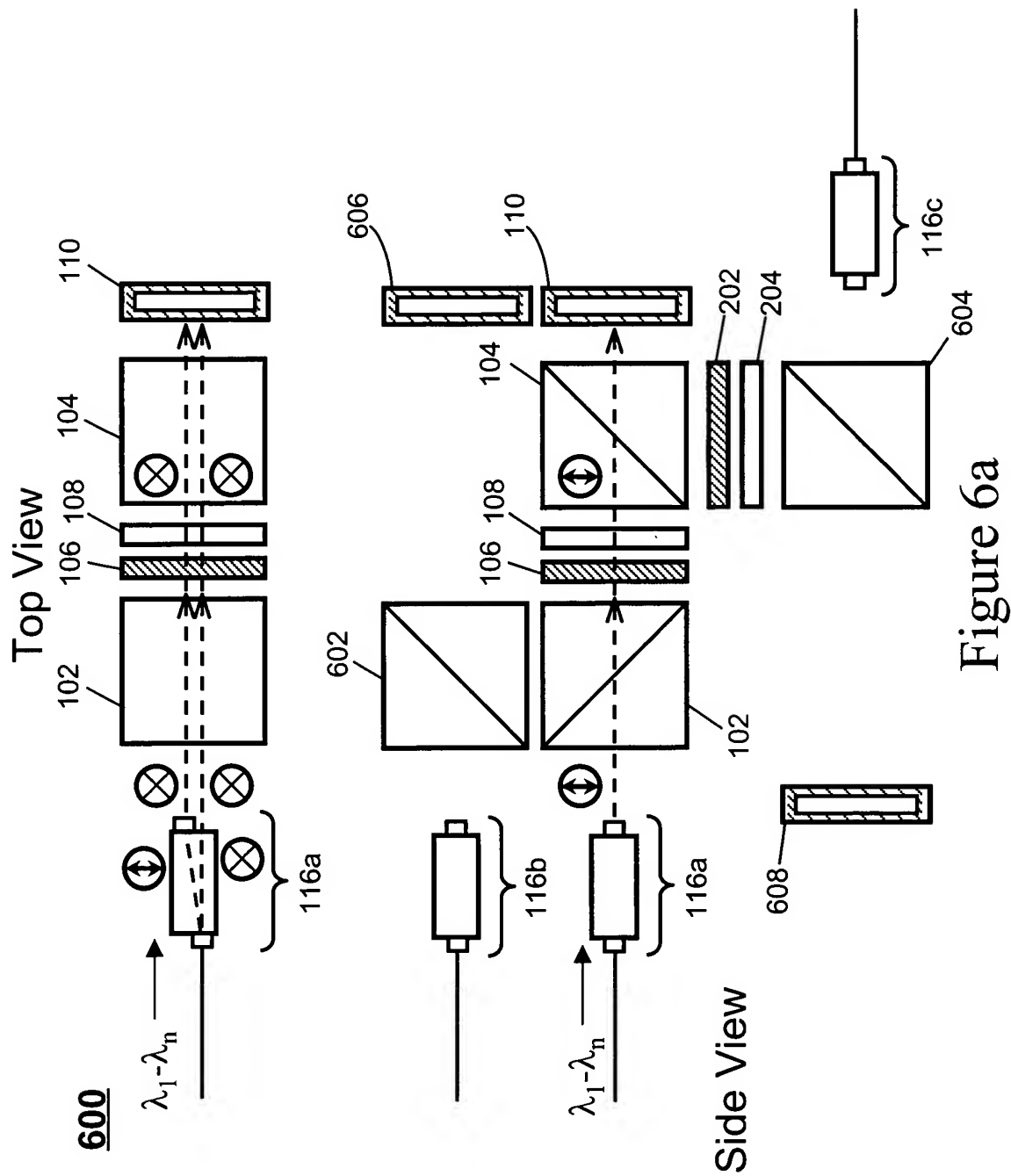
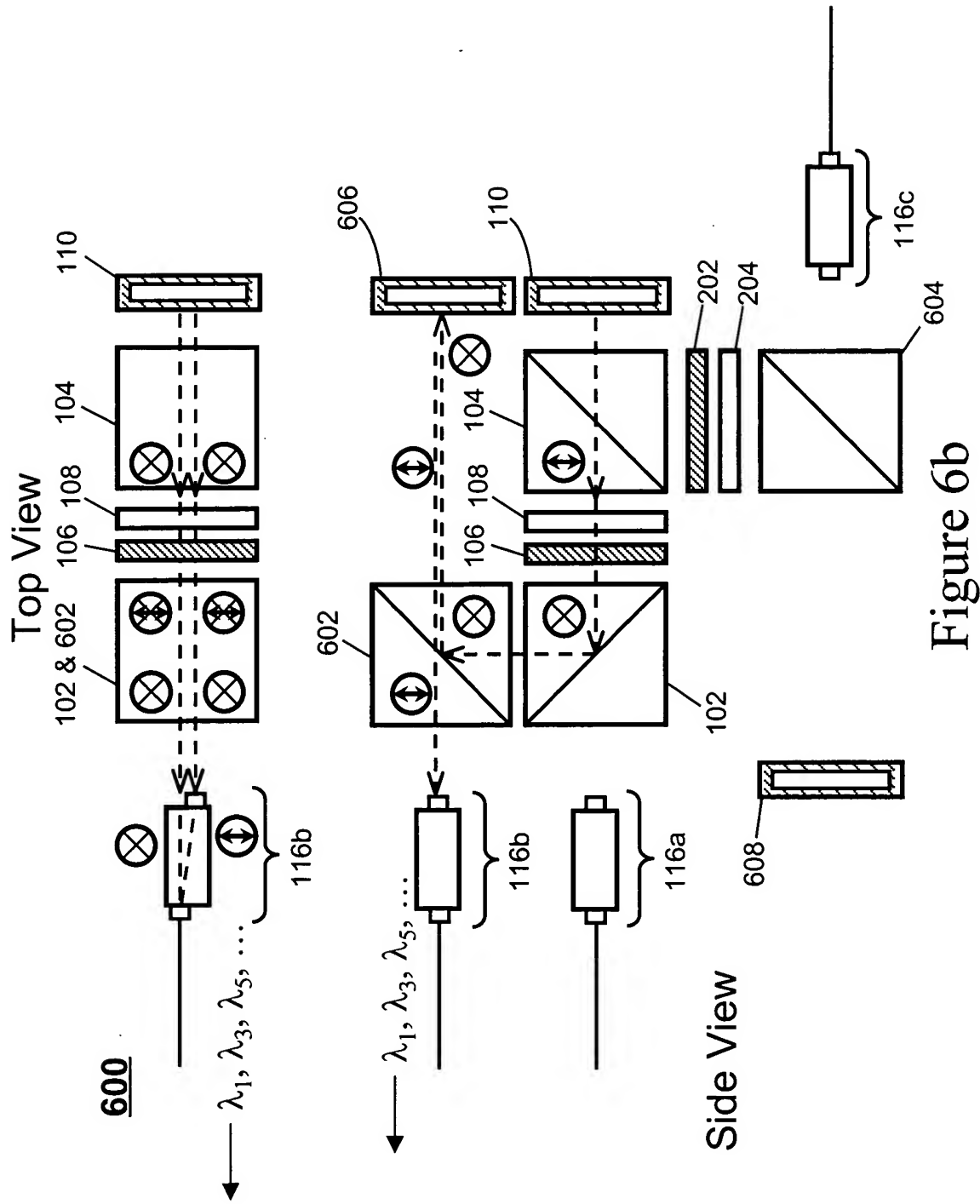


Figure 5c





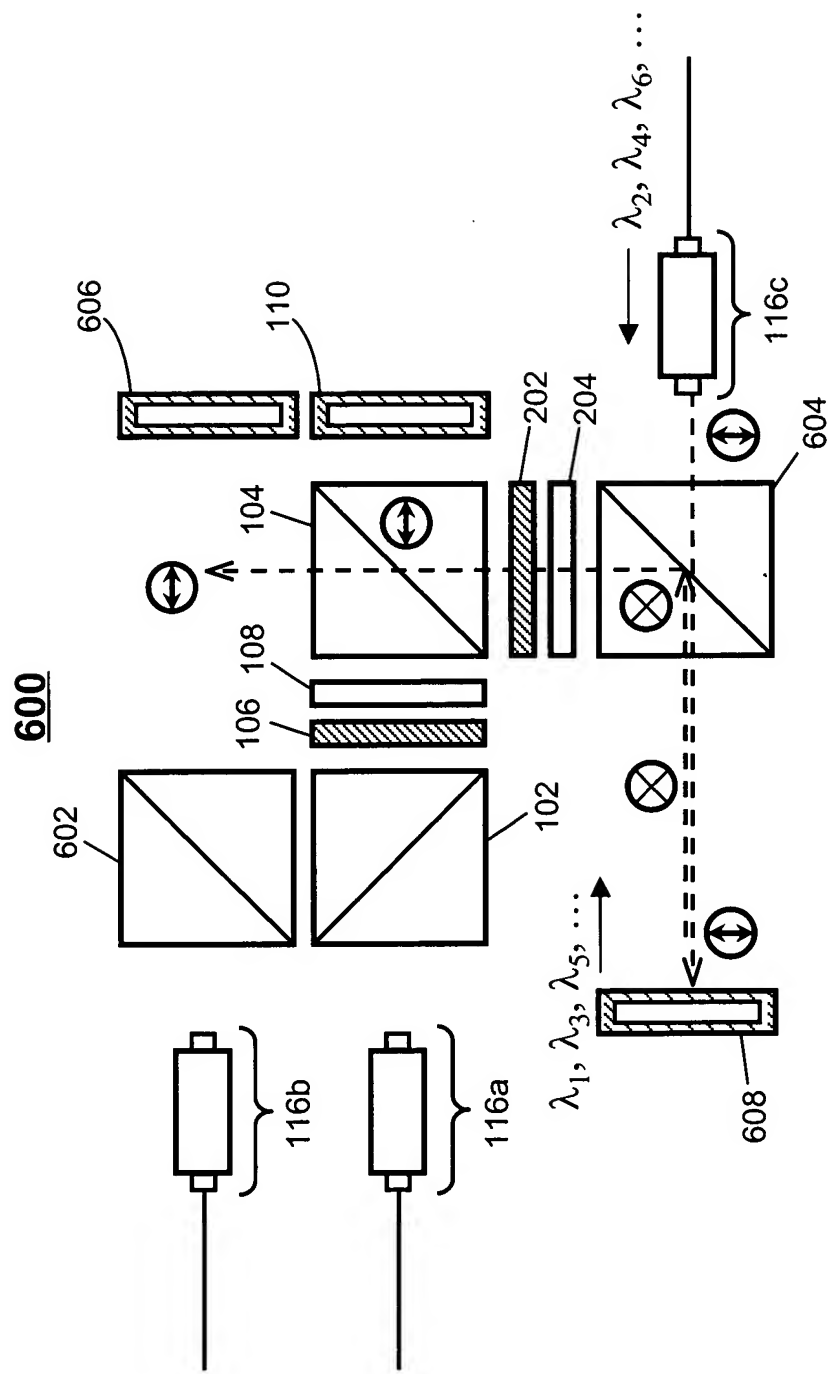


Figure 6d

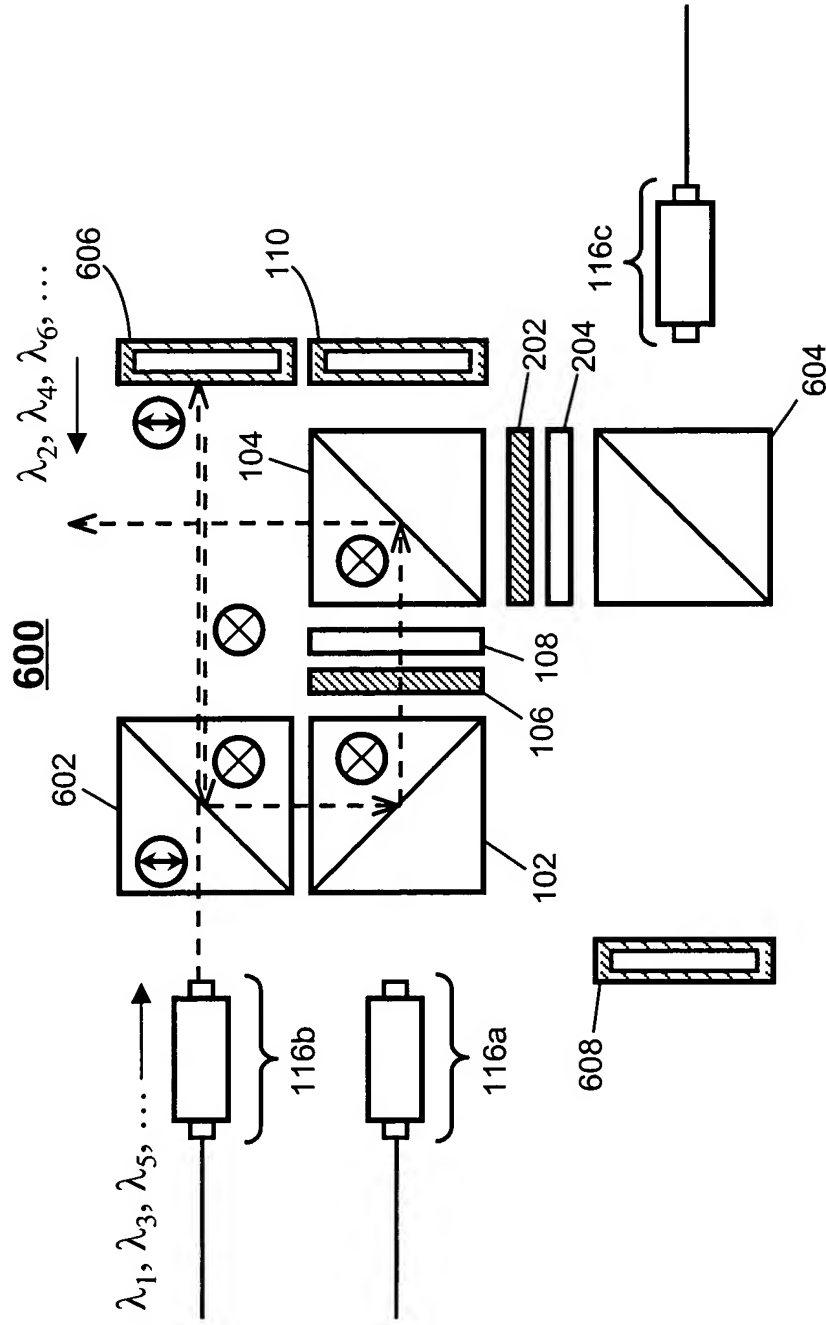


Figure 6e

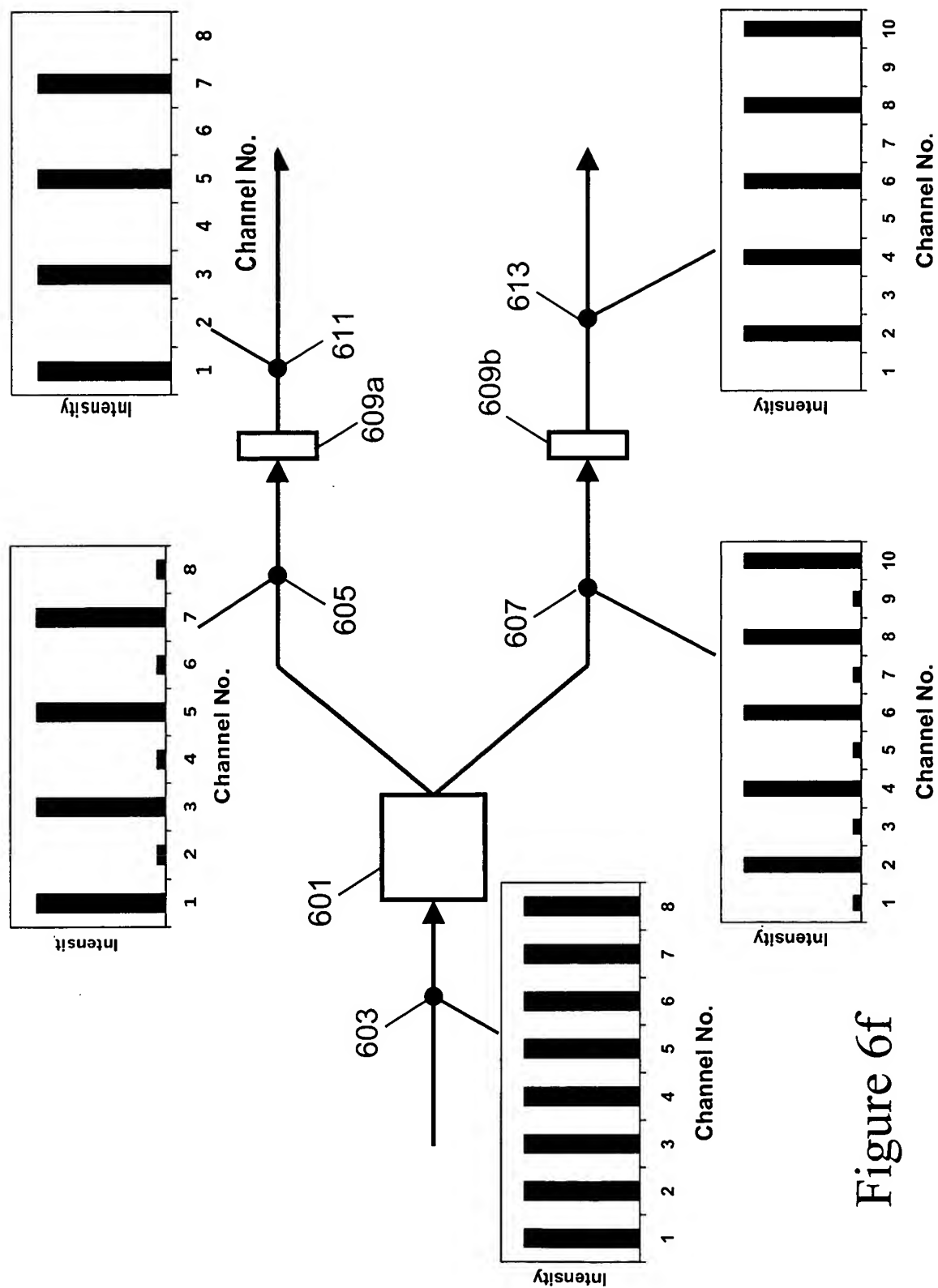


Figure 6f

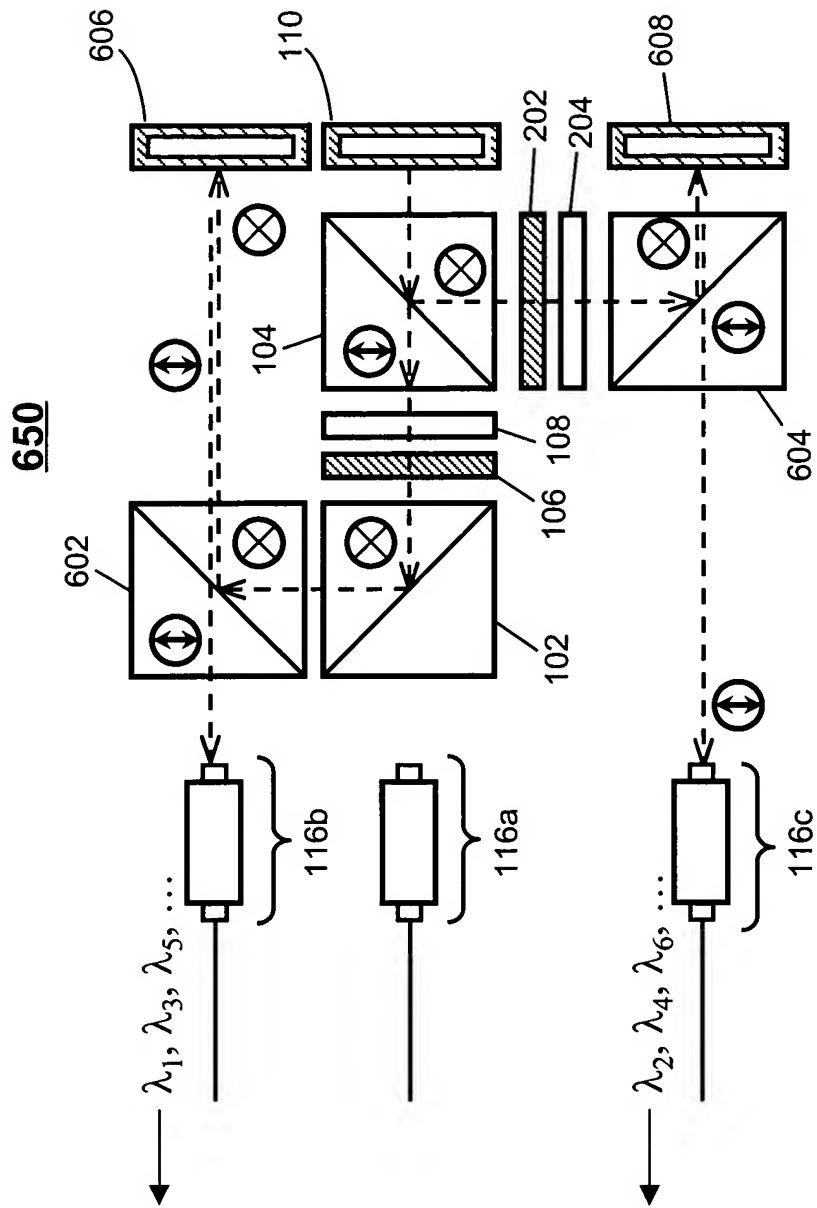


Figure 6g

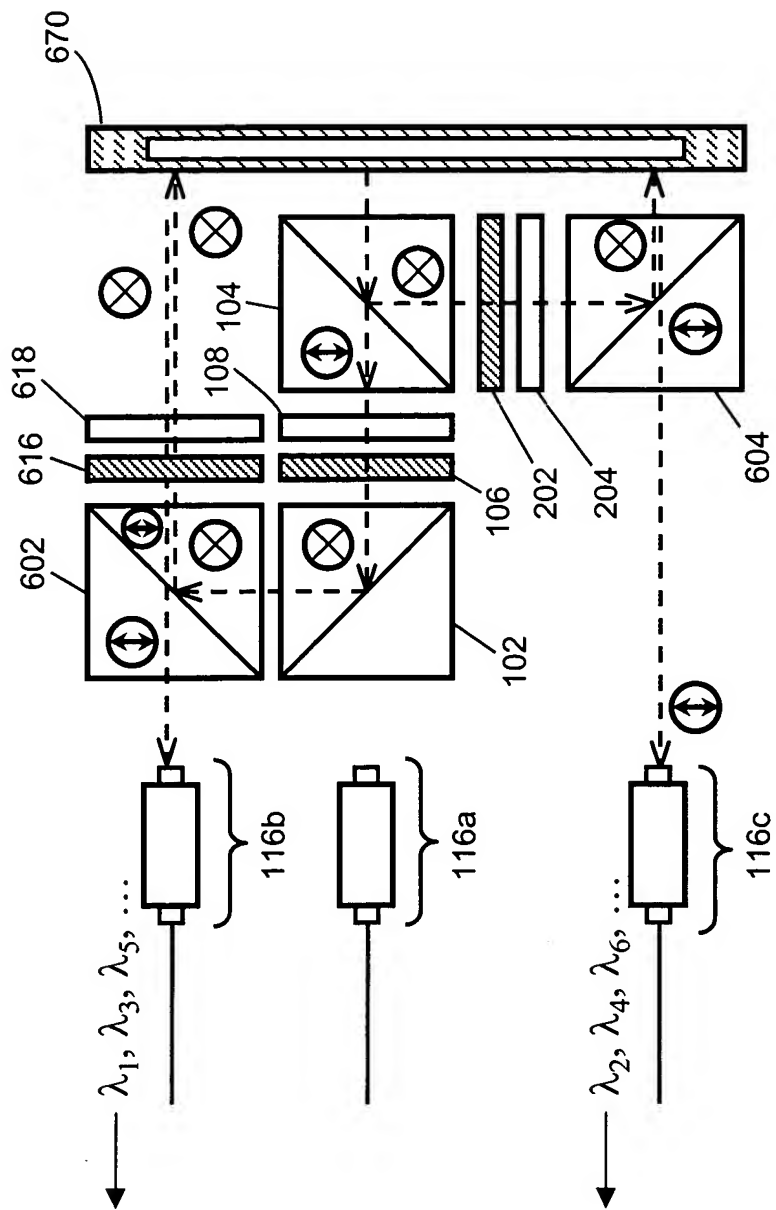
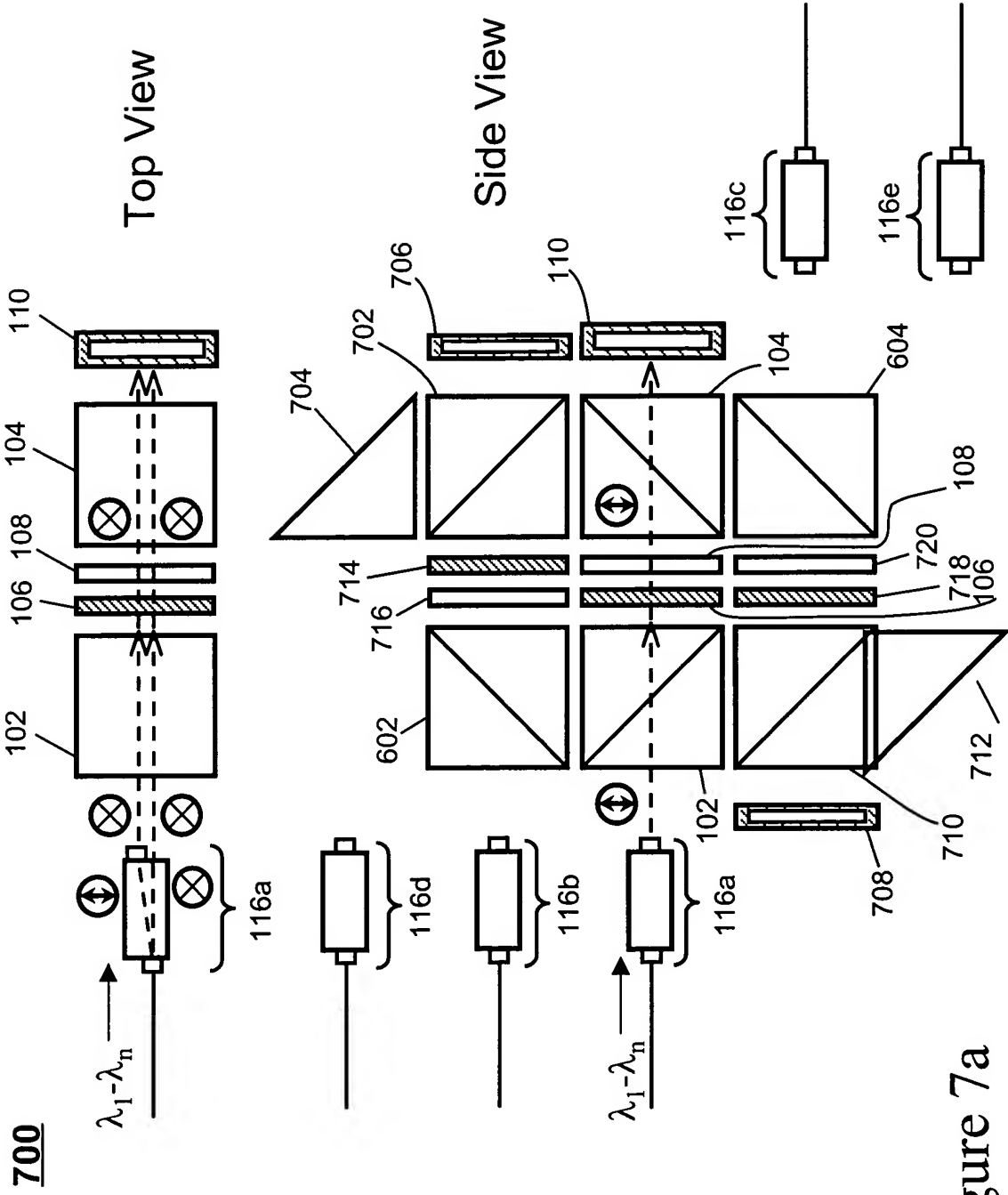


Figure 6h



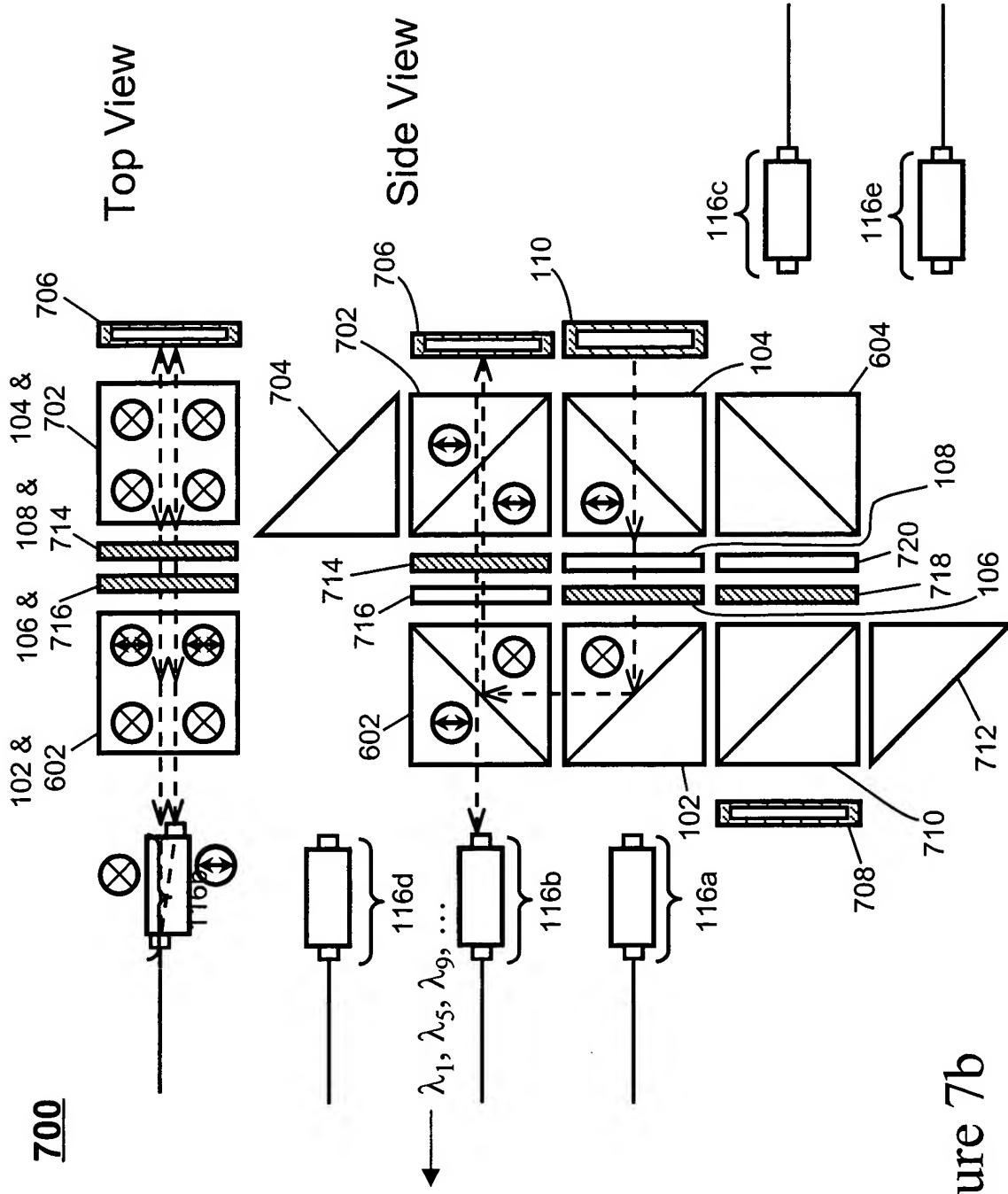


Figure 7b

700

Top View

Side View

Figure 7e

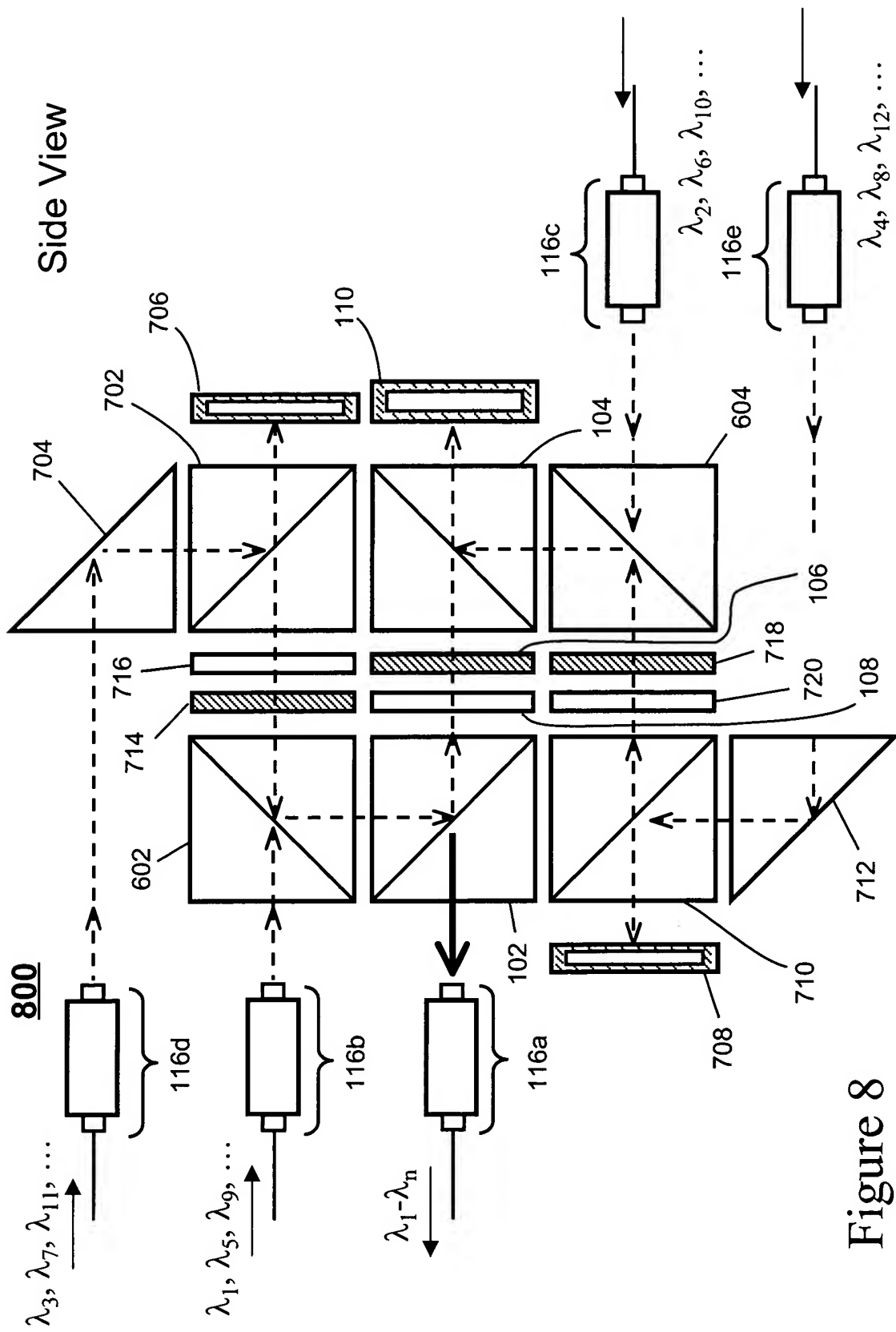


Figure 8

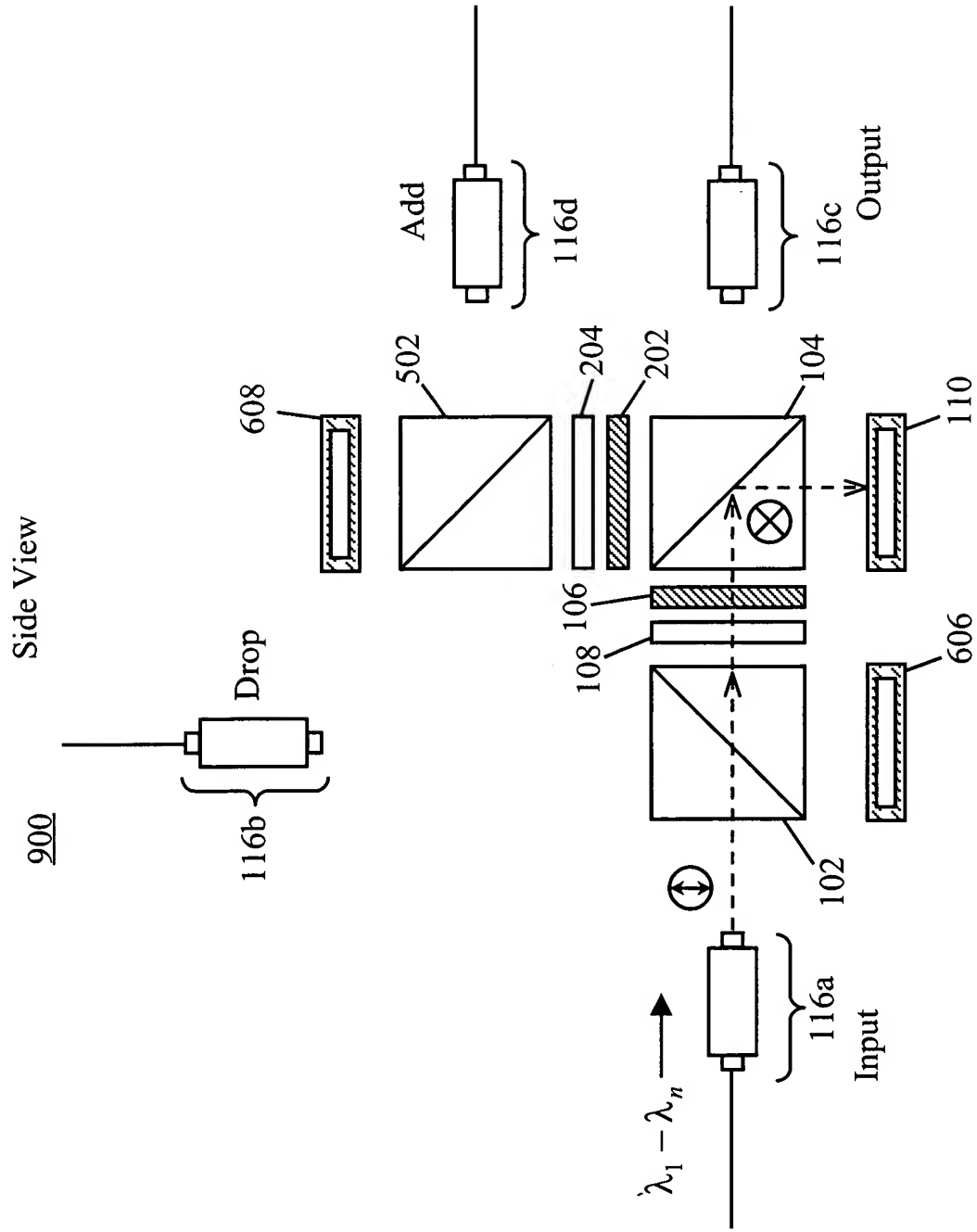


FIGURE 9A

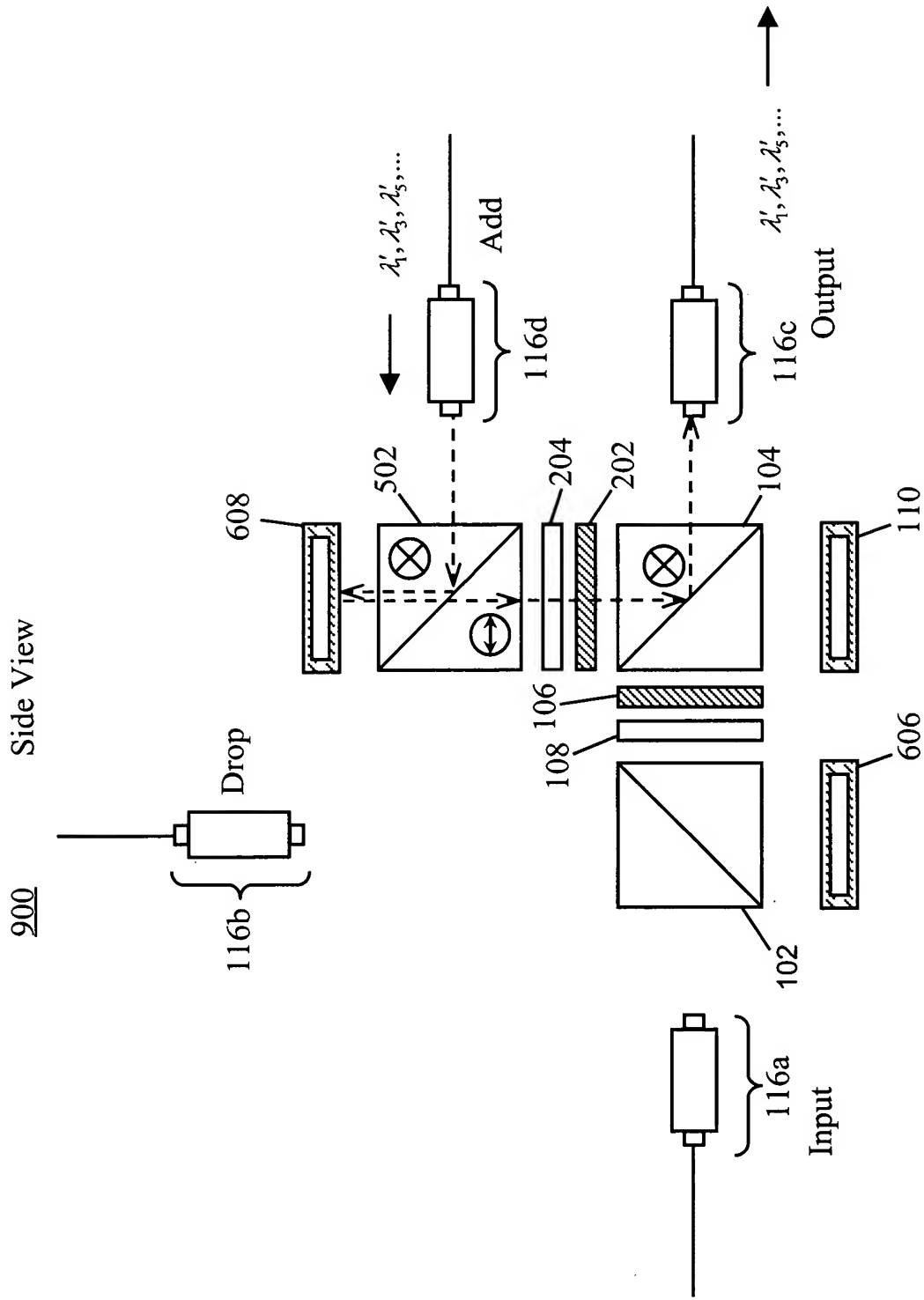
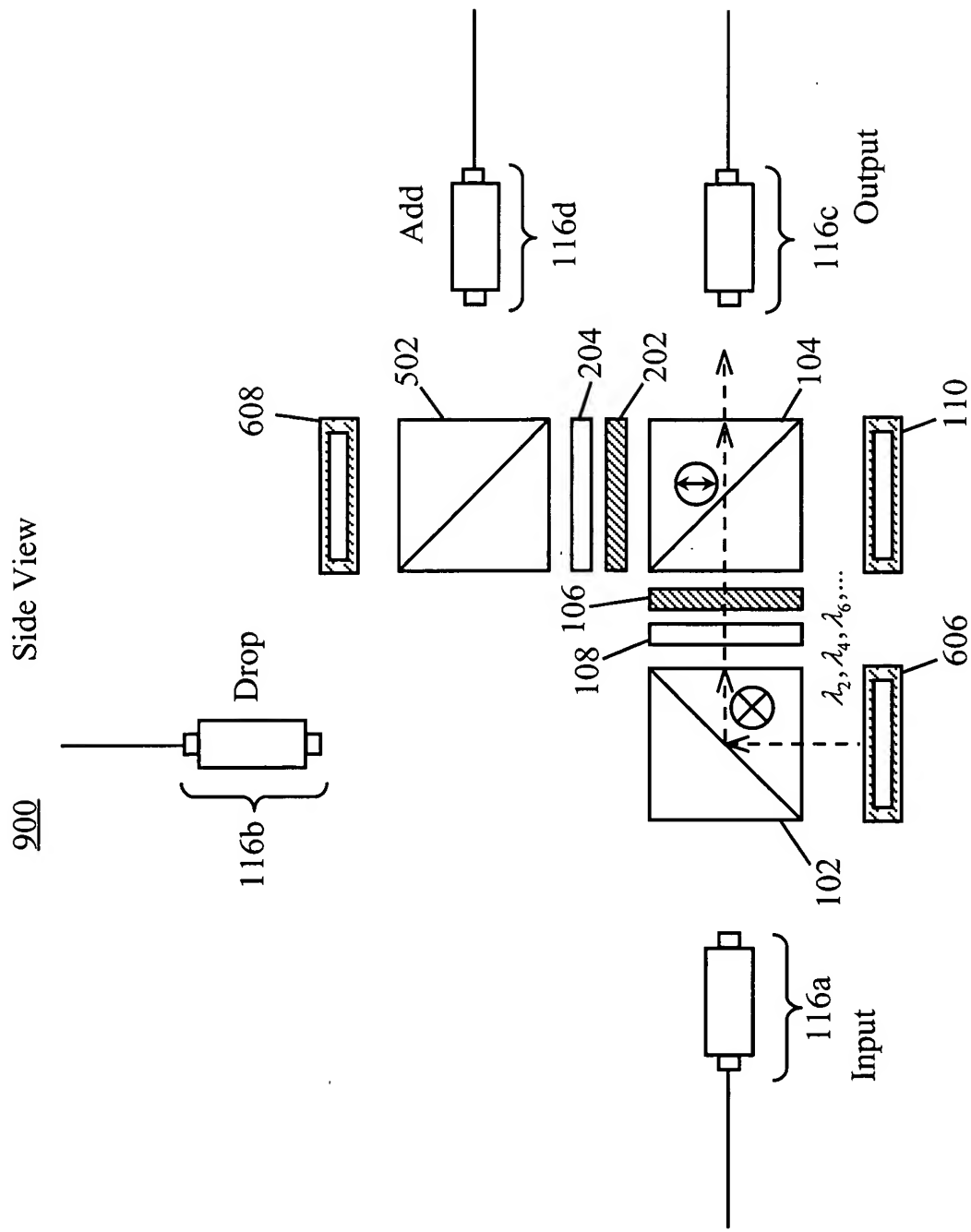


FIGURE 9C



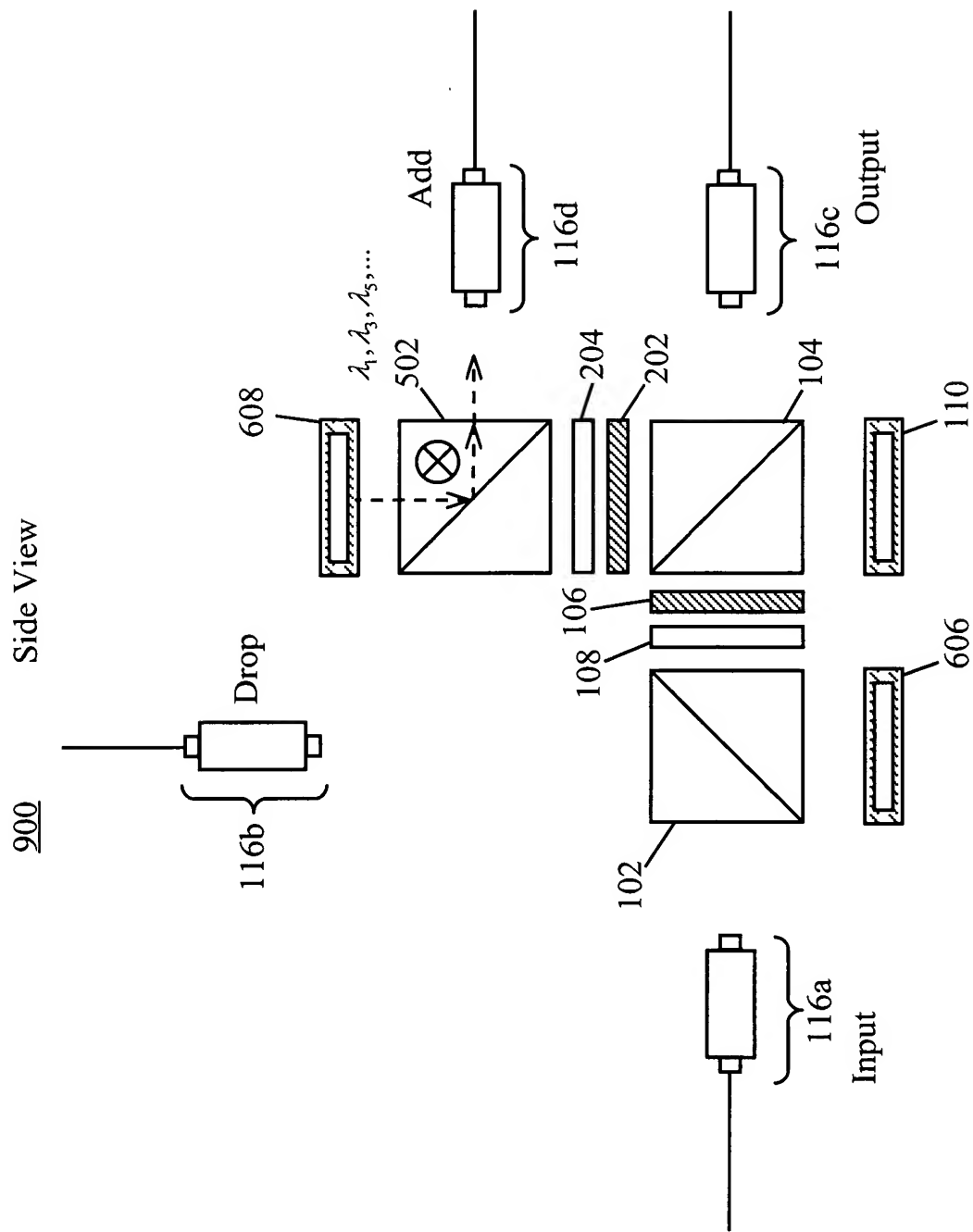


FIGURE 9E

Side View

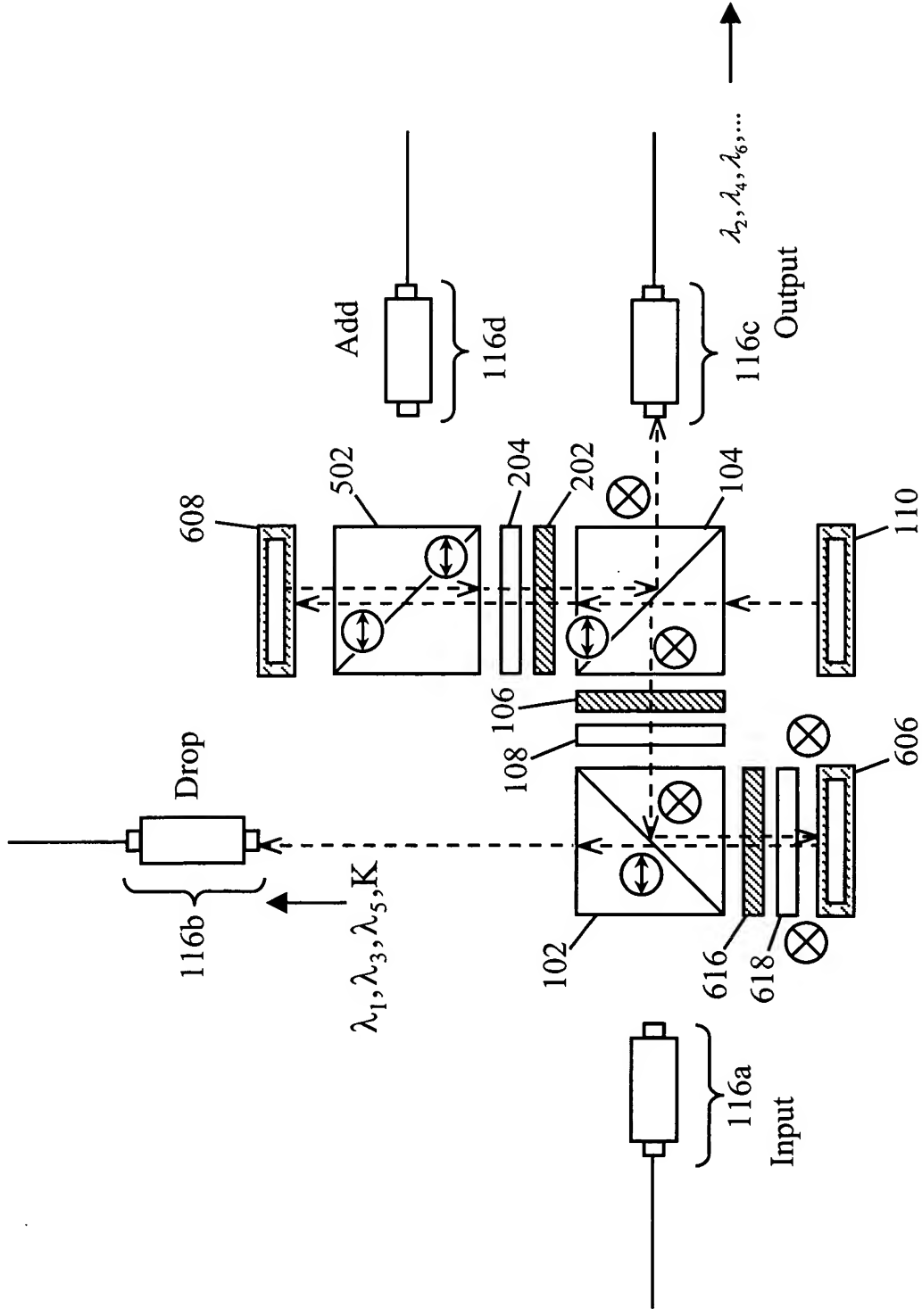


FIGURE 10A

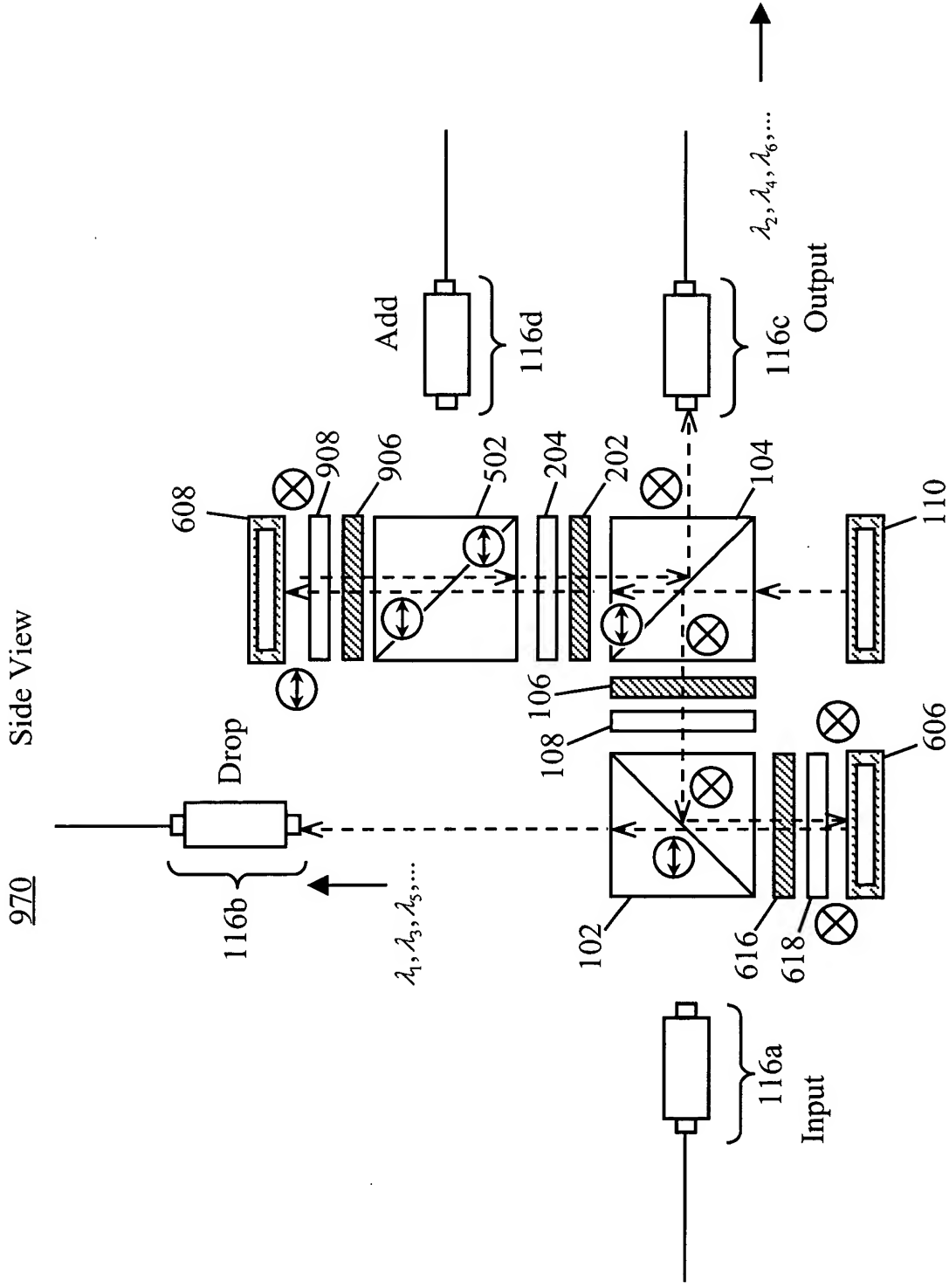


FIGURE 10B

FIG. 11 is a block diagram of a system for processing signals. The system includes an input block 116a, an add block 116d, a central processing block, a drop block 116b, and an output block 116c. The input block 116a receives a signal $\lambda_1 - \lambda_n$ and sends it to the central processing block. The add block 116d receives a signal $\lambda_1, \lambda_3, \lambda_5, \dots$ and sends it to the central processing block. The central processing block contains two paths: a solid line labeled "Even Channels" and two dashed lines labeled "Odd Channels". The output of the central processing block is sent to the drop block 116b, which then sends the signal to the output block 116c. The output block 116c outputs a signal $\lambda_1, \lambda_3, \lambda_5, \dots$.

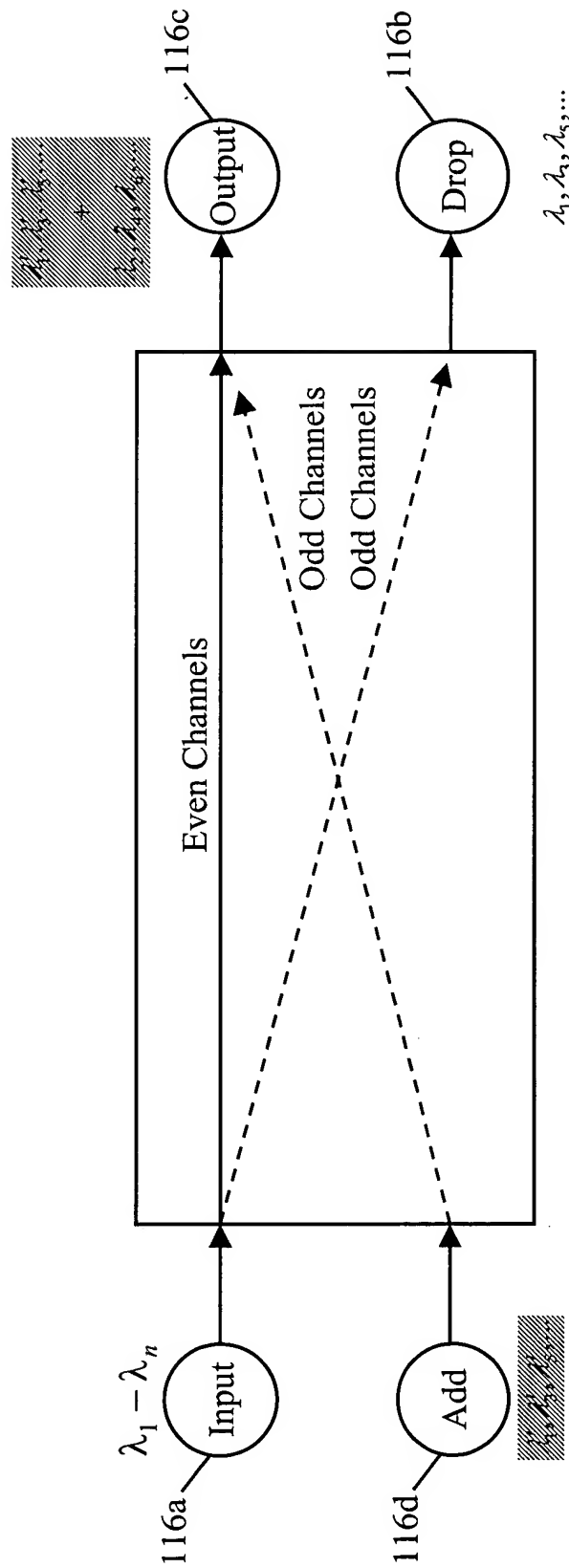


FIGURE 11